**WE CLAIM:**

1. Apparatus for processing data, said apparatus comprising:

at least one trace data source operable to generate an individual trace data stream including trace data signals and trace source identifying signals; and

a trace bus coupled to said at least one trace data source and including trace data signal lines operable to carry trace data signals and trace source identifying signal lines operable to carry trace source identifying signals.

2. Apparatus as claimed in claim 1, wherein said trace data bus includes one or more data size indicating signal lines operable to carry one or more size indicating signals indicative of how many of said trace data signal lines are carrying trace data signals.

3. Apparatus as claimed in claim 1, comprising:

a plurality of trace data sources operable to generate respective individual trace data streams each including trace data signals and trace source identifying signals;

a trace data stream combiner operable to receive and to combine said individual trace data streams to form a combined trace data stream including trace data signals and trace source identifying signals, wherein

a plurality of trace buses, each including said trace data signal lines and said trace source identifying signal lines, respectively couple said trace data sources to said trace data stream combiner and carry said combined trace data stream from said trace data stream combiner.

4. Apparatus as claimed in claim 3, wherein said combined trace data stream is coupled as an input to a further trace data stream combiner to be combined with one or more further trace data streams.

5. Apparatus as claimed in claim 1, comprising a trace data stream replicator operable to receive a single input trace data stream as an input and to replicate said single trace data stream to form a plurality of output trace data streams.

6. Apparatus as claimed in claim 5, wherein said plurality of output trace data streams are subject to different post-replication trace data stream processing.

7. Apparatus as claimed in claim 6, wherein said apparatus is an integrated circuit and one of said output trace data streams is directed to an off-chip output port and one of said output trace data streams is directed to an on-chip memory.

8. Apparatus as claimed in claim 1, comprising a trace data filter operable to perform trace data filtering in dependence upon said trace source identifying signals.

9. Apparatus as claimed in claim 7, comprising a trace data filter operable to perform trace data filtering upon trace data directed to said off-chip data port to form low bandwidth trace data.

10. Apparatus as claimed in claim 1, wherein a change in trace data source upon said trace bus is accompanied by a change in said trace source identifying signals and a trace data header is output upon said trace data signal lines at a predetermined time following a change in trace data source, whereby a change in trace source identifying signals serves as a marker indicative of a position of a trace data header.

11. Apparatus as claimed in claim 1, wherein said trace source comprises a software triggered trace data generator operable such that a software controlled write to one or more predetermined memory location triggers generation of a trace data stream by said software triggered trace data generator.

12. Apparatus as claimed in claim 1, wherein said trace data source includes one of:

a processor core;
a digital signal processor; and
a memory bus monitor.

13. Apparatus as claimed in claim 1, wherein said apparatus comprises an integrated circuit.

14. Apparatus as claimed in claim 1, wherein said trace bus includes a trace data valid signal line operable to carry a valid signal generated by said trace data source and indicative of said trace data source being active to generate said trace data signals.

15. Apparatus as claimed in claim 1, wherein said trace bus includes a trace data receiver ready signal line operable to carry a ready signal generated by a trace data receiver coupled to said data bus and indicative of said trace data receiver being active to receive said trace data signals.

16. A method of processing data, said method comprising the steps of:

generating at least one individual trace data stream including trace data signals and trace source identifying signals using a respective trace data source;

carrying trace data signals upon trace data signal lines of a trace data bus; and

carrying trace source identifying signals upon trace source identifying signal lines of said trace bus.

17. A method as claimed in claim 16, comprising carrying one or more size indicating signals lines upon data size indicating signal lines of said trace bus, said size indicating signals being indicative of how many of said trace data signal lines are carrying trace data signals.

18. A method as claimed in claim 16, comprising:

generating a plurality of individual trace data streams each including trace data signals and trace source identifying signals with respective trace data sources;

combining said individual trace data streams to form a combined trace data stream including trace data signals and trace source identifying signals upon a combined stream trace data bus.

19. A method as claimed in claim 18, wherein said combined trace data stream is combined with one or more further trace data streams.

20. A method as claimed in claim 16, comprising replicating a single trace data stream to form a plurality of output trace data streams.

21. A method as claimed in claim 20, wherein said plurality of output trace data streams are subject to different post-replication trace data stream processing.

22. A method as claimed in claim 21, wherein said method is performed upon an integrated circuit and one of said output trace data streams is directed to an off-chip output port and one of said output trace data streams is directed to an on-chip memory.

23. A method as claimed in claim 16, comprising filtering trace data in dependence upon said trace source identifying signals.

24. A method as claimed in claim 22, comprising filtering trace data directed to said off-chip data port to form low bandwidth trace data.

25. A method as claimed in claim 16, wherein a change in trace data source upon said trace bus is accompanied by a change in said trace source identifying signals and a trace data header is output upon said trace data signal lines at a predetermined time following a change in trace data source, whereby a change in trace source identifying signals serves as a marker indicative of a position of a trace data header.

26. A method as claimed in claim 16, wherein a software controlled write to one or more predetermined memory location triggers generation of a trace data stream by a software triggered trace data generator.

27. A method as claimed in claim 16, wherein said trace data source includes one of:

a processor core;
a digital signal processor; and
a memory bus monitor.

28. A method as claimed in claim 16, wherein said method is performed upon an integrated circuit.

29. A method as claimed in claim 16, comprising carrying a valid signal upon a trace data valid signal line of said trace data bus, said valid signal being indicative of said trace data source being active to generate said trace data signals.

30. A method as claimed in claim 16, comprising carrying a trace data receiver ready signal upon a trace data receiver ready signal line of said trace data bus, said trace data receiver ready signal being indicative of said trace data receiver being active to receive said trace data signals.